Introduction to Digital Logic

EECS/CSE 31L

**Assignment 4 Design Report**

**Designing Register**

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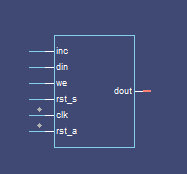
1 BLOCK Description

This 32-bit register is designed to receive a 32-bit input and read out the 32-bit input as the 32-bit output if write enable is active. It supports asynchronous and synchronous resets, meaning when the asynchronous signal is enabled, the output will be 0 whether the clock signal is on or off and when the synchronous signal is enabled, the out should be 0 only when the clock signal is on. This design also features an incrementing feature, which increments the output by one.

2 Input/Output Port Description

|  |  |  |  |
| --- | --- | --- | --- |
| Port Name | Port Size | Port Type | Description |
| clk | 1 | IN | Clock Signal |
| rst\_a | 1 | IN | Asynchronous Reset Signal |
| rst\_s | 1 | IN | Synchronous Reset Signal |
| inc | 1 | IN | Increment Signal |
| we | 1 | IN | Write Enable Signal |
| din | 32 | IN | 32-bit Input |
| dout | 32 | OUT | 32-bit Output |

3 Design Schematic



4 Wave Map

